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Low Power And Low Area Alu Design Using Gdi (Gate Diffusion Input)Technique

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ABSTRACT:- Rapid development of portable digital applications, the demand for increasing speed, compact implementation, and low power dissipation triggers numerous research efforts. The wish to improve the performance of logic circuits, once based on traditional CMOS technology, resulted in the development of many logic design techniques during the last two decades. GDI (Gate diffusion input) a technique of low power digital combinational design. This technique as compare to other currently used logic design styles, allows less power consumption and reduced propagation delay for low -power design of combinatorial digital circuits with minimum number of transistors.In this paper presented with 4-bit arithmetic logical unit design with the use of Gate Diffusion Input Technique. And the ALU consist of 2*1 and 4*1 and full adder implementations.system robustness.

Keywords:- Double fed induction wind generators, direct power control, microgrid, robustsliding mode control, voltage regulation.

I. INTRODUCTION

A processor is a main part of any digital system. Andan ALU is one of the main components of a microprocessor. To give a simple analogy, CPU works as abrain to any system & and ALU works as a brain toCPU. So it's a brain of computer's brain. They areconsists of fast dynamic logic circuits and havecarefully optimized structures. Of total powerconsumption in any processor, CPU accounts asignificant portion of it.ALU also contribute to one of the highest powerdensity locations on the processor, as it is clocked atthe highest speed and is busy mostly all the timewhich results in thermal hotspots and sharptemperature gradients within the execution core.Therefore , this motivate us strongly for a energyefficient ALU designs that satisfy the highperformance requirements, while reducing peak andaverage power dissipation.[1,2] Basically ALU is acombinational circuit that performs arithmetic andlogical operations on a pair of n bit operands e.g. A[0:7] & B [0:7] for 8 bits.

•The arithmetic logic circuits are to be designed with compact size, less power and propagation delay.
•Arithmetic operations are indispensable and basic functions for any high speed low power application digital signal processing, microprocessors, image processing etc.
•Addition is most important part of the arithmetic unit rather approximately all other arithmetic operation includes addition. Thus, the primary issue in the design of any arithmetic logic unit is to have low power high performance adder cell.
•There are various topologies and Methodologies proposed to design full adder cell efficiently. This paper utilizes the concept of GDI technique in the design of ALU and its sub blocks as Multiplexer and Full adder.

The typical internal structure of a 8 bit ALU is shownin Fig.1. The architecture can be modified similarlyfor lower bits. Our work is divided into followingsections: Section (II) give description of various unitsand operations of ALU, Section (III) briefly presentsthe designing of various ALU components such asShifter, adder, subtractor etc. using conventionalcomplementary design.

A. ARITHMETIC LOGIC UNIT

1.1Arithmetic Unit

Employing fast and efficient adders in arithmetic logicunit will aid in the design of low power highperformance system. Other operations such assubtraction and multiplication also employ addition intheir operations, and their internal hardware is almostsimilar though not identical to addition hardware.Various adder families have been proposed in the pastto trade-off power, area and speed for possible use inALUs. The performance criticality of the ALUdemands a dynamic adder implementation. Dynamiclogic family of adders are the most efficient in termsof transistor-count, speed and power dissipation. Thiswork covers the design of 3

bit adder usingComplementary logic. This same Adder unit is usedfor the implementation of subtractor unit. This reusesthe current hardware we made for adder and savesarea.

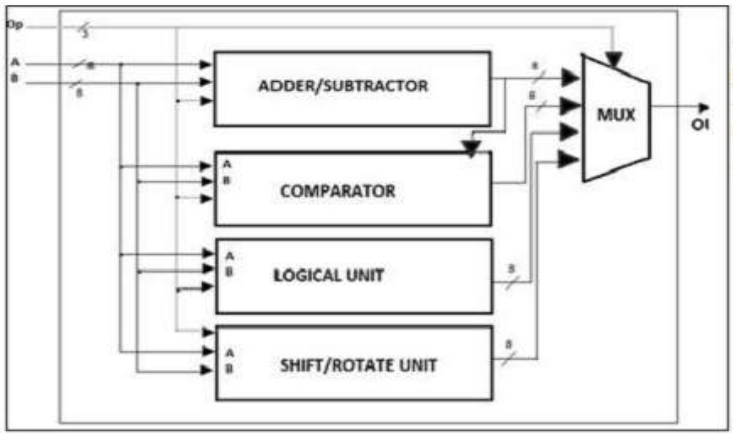


Fig.1 Internal Architecture of ALU

1.2 Logic Unit

ALU can perform various logic operations like NOT,AND, OR, NAND, NOR, XOR, XNOR etc. For theseoperations a special unit is made called as LogicalUnit. This Logic Unit performs all logic operationsasked to perform. A MUX operated by select lines,for which particular logic operation to perform, isused inside this logic block.

1.3 Comparator & Shifter unit

A 1-bit comparator is made with the help ofComplementary logic. It compare the two I/Ps andgive three states of O/P for three different conditions.Also a 2:1 MUX is made which is used as a cell in thebarrel shifter. Used for shifting and rotating operation.

1.4 Low Power ALU using 4:1 MUX

There is a substantial increase in the standby mode leakage power, When technology is scaled from say250nm to 180nm. Reducing the power consumption ofthe ALU of high-end processors is important not onlybecause they consume a considerable percentage ofprocessor energy, but also because they are one of themost active and busiest component of the processor.As a result of they dissipate a lot of dynamicenergy. This is aggravated by the exponentialdependence of leakage on the temperature, & ALUalso become a site of high leakage. The total leakageof the ALU can be given as

IS,T=N.IS,i

Where, N= number of transistors in the ALU

IS,i= sub threshold leakage of gate i which is afunction of gate length L.

Similarly, the dynamic power of the ALU is given asID=α.Ceff.Vdd2.f

where α is the switching factor , Ceff. is the total effective capacitance,Vdd is the supply voltage& f is the frequency of operation.

II. RELATED WORKS

•There are different types and designs of full adder which is discussed in various papers at state of the art level and process and circuit level. Twelve state of the art full adder cells are: conventional CMOS, CPL, TFA, TG CMOS, C2MOS, Hybrid, Bridge, FA24T, N-Cell, DPL and Mod2f.

•R. Shalem, E. John, and L.K. John, proposed a conventional CMOS full adder consisting of 28 transistors . Later, the number of transistor count is reduced to have less area and power consumption.

• A. Sharma, R Singh and R. Mehra, Member, IEEE, have improved performance with Transmission Gate Full adder using CMOS nano technology where 24 transistors are used.

•The Complementary Pass-transistor Logic (CPL) full Adder contains the 18 transistors. The power consumption of this structure is 2.5μw.

•A Transmission Function Full Adder (TFA) based on the transmission function theory has 16 transistors. The power consumption of this structure is 12μw.

•N-CELL contains the 14 transistors and utilizes the low power XOR/XNOR circuit. The power consumption of this structure is 1.62μw.

•Mod2f Full Adder contains the 14 transistors, generates full swing XOR and XNOR signals by utilizing a pass transistor based DCVS circuit. The power consumption of this structure is 2.23μw.

•Saradindu Panda, N. Mohan Kumar, C.K. Sarkar, optimized the full adder circuit to 18 Transistor using Dual Threshold Node Design with Submicron Channel Length.
•T. Vigneswaran, B. Mukundhan, and P. Subbarami Reddy, designed 14 transistor high speed CMOS full adder and significantly improved threshold problem to 50%.
Gate Diffusion Input Technique is a new method of reducing power dissipation, propagation delay with less area. We have designed ALU in different way by using GDI cells to implement multiplexers and full adder circuit. The input and output sections consist of 4x1 and 2x1 multiplexers and ALU is implemented by using full adder.Ex: T. Esther Rani, M. Asha Rani, Dr. Rameshwar Rao, designed an area optimized low power arithmetic and logic unit in which Arithmetic Logic Unit is implemented using logic gates, pass transistor logic, as well as GDI technique.

III. PROPOSED SYSTEM STRUCTURE

An arithmetic logic unit (ALU) is a fundamental building block of the Central Processing Unit (CPU) of a computer, and even the simplest microprocessors contain one. It is responsible for performing arithmetic and logic operations such as addition, subtraction, increment, decrement, logical AND, logical OR, logical XOR and logical XNOR.ALU consists of eight 4x1 multiplexers, four 2x1 multiplexers and four full adders. The 4-bit ALU is designed in 250nm, n-well CMOS technology. When logic '1'and logic '0' are applied as an input INCREMENT and DECREMENT operations takes place respectively. An INCREMENT operation is analyzed as adding '1' to the addend and DECREMENT is seen as a subtraction operation [6]. Two's complement method is used for SUBTRACTION in which complement of B is used. The outputs obtained from the full adder are SUM, EXOR, EXNOR, AND & OR.

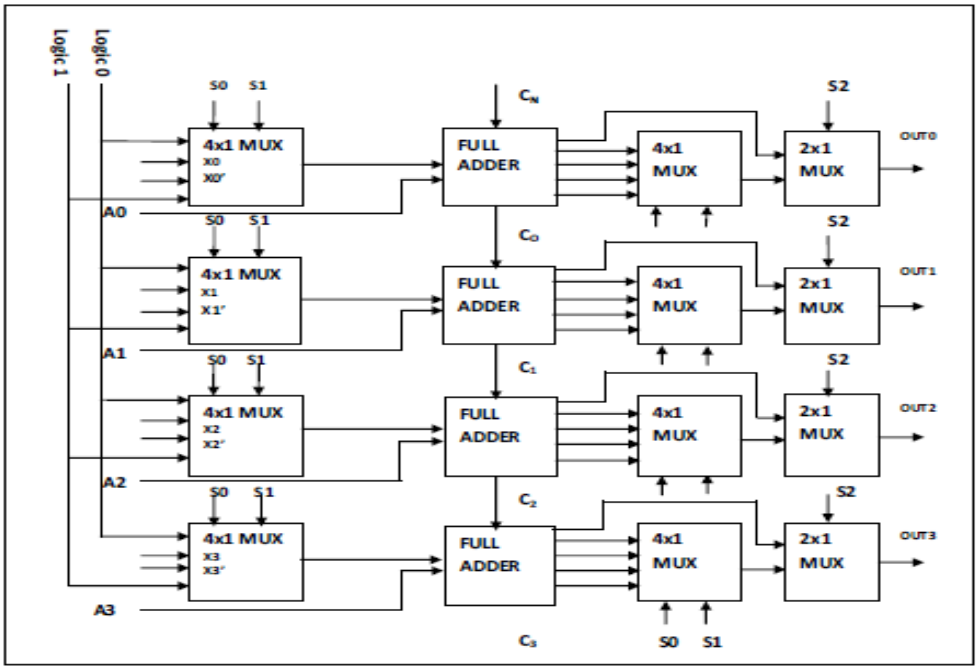


Fig. 2. 4-bit Arithmetic and Logic Unit

Fig:2 shows the block diagram of 4-bit ALU where the first stage to fourth stage is cascaded with the CARRY bit. Symbolic representation of 4-bit ALU has been visualized in fig. 3.The multiplexer stage selects the appropriate inputs based on the condition of the select signals, and gives it to the full adder which then computes the results.The multiplexer at the output stage selects the appropriate output and route it to output port. The operation being performed and the inputs and outputs being selected are determined by set of three select signals incorporated in the design. Fig 8.shows multiplexer logic at input port and Fig 9. shows multiplexer logic at output port.The multiplexer stage selects the appropriate inputs based on the condition of the select signals, and gives it to the full adder which then computes the results. The multiplexer at the output stage selects the appropriate output and route it to output port. Table 2 shows the truth table for the operations performed by the ALU based on the status of the select signal.

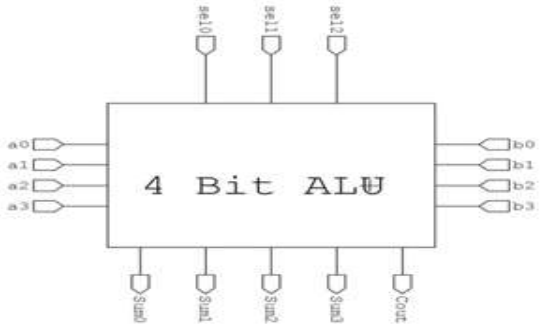
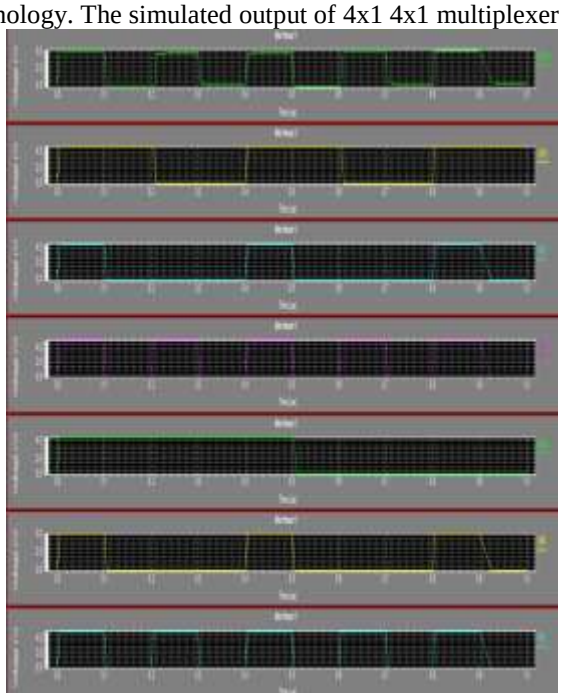


Fig 3. Symbol of 4-bit ALU

The schematic of ALU is designed using schematic editor of Tanner EDA. It shows connectivity between the components and describes aspect ratios of the transistor that can be modified along with the design. Figure 10 represents the complete schematic view of ALU. The 4-bit ALU consists of two 4-bit inputs, three selecting lines, and one carry input, one carry output and four output bits.This paper presents a new approach using concept of Gate Diffusion Input Technique to design an arithmetic and logic unit. In an ALU, for appropriate selection of input to perform particular operation and for obtaining output accordingly multiplexer is the most applicable device. In earlier designs of ALU, the multiplexer unit is either implemented by conventional CMOS logic or by pass transistor logic which proven to have high power consumption. The approach gives better result than previous designs in terms of power consumption, propagation delay as well as area.

IV. SIMULATION RESULTS

This section describes performance of the proposed design using Tanner EDA tool on 250nm technology. The simulated output of 4x1 4x1 multiplexer and full adder is shown in Figure 4.



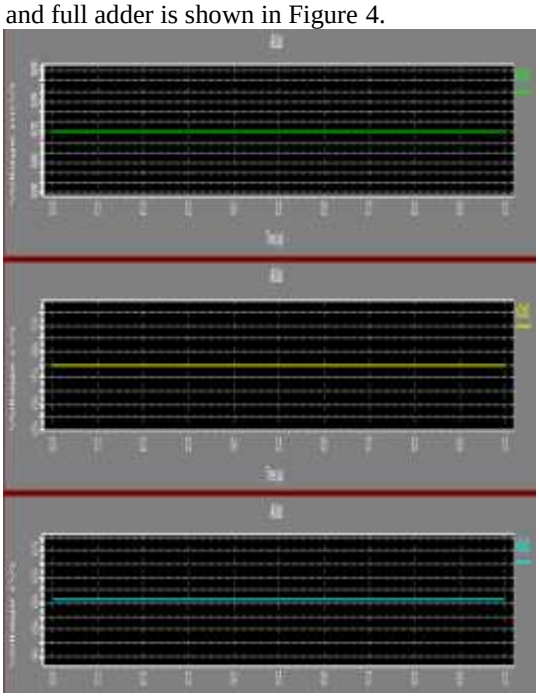


Fig :4 Waveform for 4X1 multiplexer using six transistors **Fig : 5 Waveform for ALU**

The number of transistor required and power consumption for the individual cells of the ALU is listed in Table I and the total power consumption and number of transistor of the ALU designed in different ways is listed in Table II.

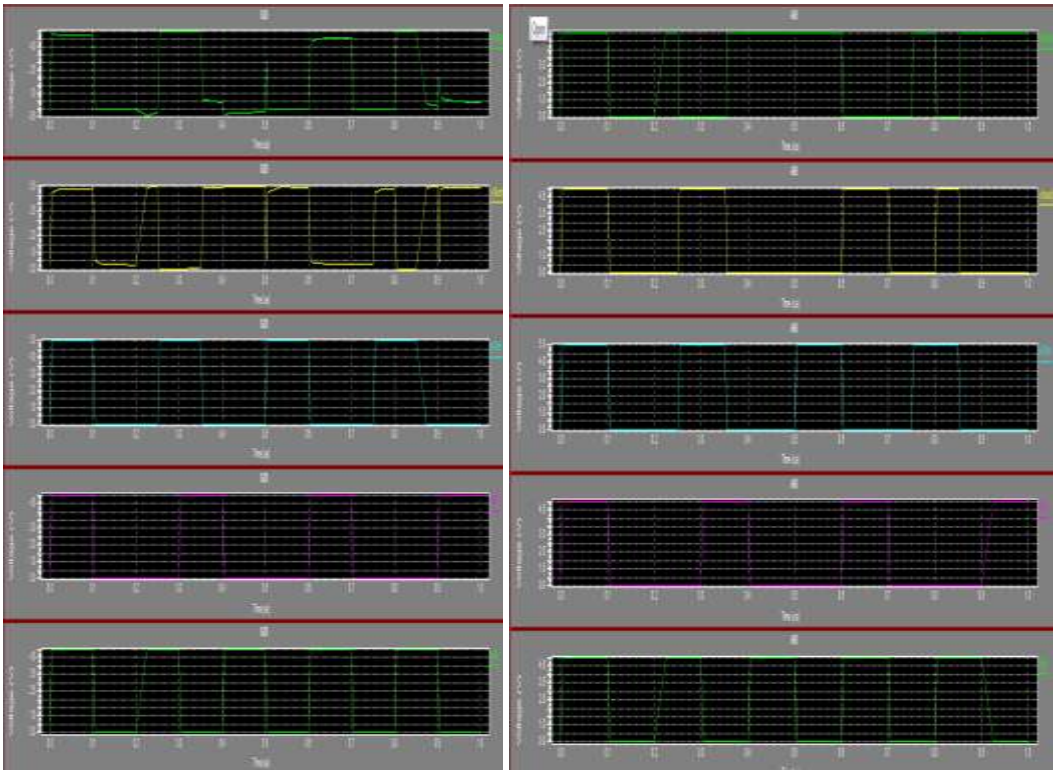


Fig :6Waveform for GDI(Gate diffusion input) Fig : 7 Waveform for Proposed GDI(Gate diffusion input)

Table i. Analysis result of different block of alu

S. No.	Design	Cell	Power (µW)	No. of Trans-istor
1	CMOS	2x1 MUX	4.6073	6
2		4x1MUX	15.123	18
3		Conventiona l Full adder	16.675	28
4	Pass Transistor Gate	2x1 MUX	1.6079	4
5		4x1MUX	4.225	8
6		Full adder	11.998	24
7	GDI	2x1 MUX	1.394	2
8		4x1MUX	2.987	6
9		Full adder	10.190	10

S.No.	Design	No. of Transistors	Power(µW)
1	ALU with CMOS Gate	592	4204.5
2	ALU with transmission Gate and 10 Transistor full adder	416	1197.5
3	Proposed ALU with GDI based Full adder	232	1030.5

TABLE II. POWER CONSUMPTION OF 4-BIT ALU

V. CONCLUSION

Power consumption in CMOS circuit is classified in two categorize: static power dissipation and dynamic power dissipation. In today's CMOS circuits static power dissipation is negligible thus not considered as compared to dynamic power dissipation. Dynamic Power dissipation in a CMOS circuit is given by P = CLf VDD2. The power supply is directly related to dynamic power. The numbers of power supply to ground

connections are reduced in GDI implementation which reduces the dynamic power consumption. This work presents a 4-bit ALU designed in 250nm technology for low power and minimum area with GDI technique. Various topologies of multiplexer and full adder implementation is studied and compared. The 2x1 multiplexer, 4x1 multiplexer, 1-bit full adder with 10- transistors designed using GDI technique is chosen for lowering power consumption and minimum possible area. Power dissipation, propagation delay and the number of transistors of ALU were compared using CMOS, nMOS PTL and GDI techniques. GDI technique proved to have best result in terms of performance characteristics among all the design techniques.

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P. Rahul Reddy attained his B.Tech in Electronics & Communication Engineering and M.Tech in the stream of Embedded Systems from JNTU, Hyderabad. He is having teaching experience of more than 5 years in various Under Graduate and Post Graduate course. He has guided lots of students in various Under Graduate and Post Graduate Research Projects. At present, he is working as Associate Professor, Department of ECE in Swami Ramananda Tirtha Institute of Science & Technology, Nalgonda, India.